

WHAT IS CLAIMED IS:

1        1. A thin film transistor array panel comprising:  
2              a gate line formed on an insulating substrate;  
3              a gate insulating layer on the gate line;  
4              a semiconductor layer on the gate insulating layer;  
5              a data line formed on the gate insulating layer;  
6              a drain electrode formed at least in part on the semiconductor layer;  
7              a color filter formed on the data line and the drain electrode;  
8              a first passivation layer formed on the color filter; and  
9              a pixel electrode formed on the color filter, connected to the drain electrode, overlapping  
10         the first passivation layer, and enclosed by the first passivation layer.

1        2. The thin film transistor array panel of claim 1, wherein an overlapping portion of  
2         the first passivation layer and the pixel electrode is disposed on the data line.

1        3. The thin film transistor array panel of claim 1, wherein edges of the pixel  
2         electrode overlap the first passivation layer and the first passivation layer has an opening having  
3         edges located near the edges of the pixel electrode.

1        4. The thin film transistor array panel of claim 1, wherein the data line includes a  
2         pair of rectilinear portions connected to each other and making an angle of about 45 degrees.

1           5.     The thin film transistor array panel of claim 1, further comprising a storage  
2     electrode line formed on the substrate and including an expansion overlapping the pixel electrode  
3     to form a storage capacitor.

1           6.     The thin film transistor array panel of claim 5, wherein the drain electrode  
2     includes an expansion overlapping the expansion of the storage electrode line.

1           7.     The thin film transistor array panel of claim 1, wherein the first passivation layer  
2     comprises at least one of organic insulator and inorganic insulating material.

1           8.     The thin film transistor array panel of claim 1, wherein the first passivation layer  
2     is made of photosensitive material.

1           9.     The thin film transistor array panel of claim 1, further comprising a second  
2     passivation layer disposed between the color filters and the data line.

1           10.    The thin film transistor array panel of claim 1, wherein the second passivation  
2     layer has a contact hole exposing at least a portion of the drain electrode, the color filter has an  
3     opening disposed on the drain electrode, and the pixel electrode is connected to the drain  
4     electrode through the opening and the contact hole.

1           11.    The thin film transistor array panel of claim 1, further comprising a contact  
2     assistant formed on a portion of the gate line or a portion of the data line and made of the same  
3     material as the pixel electrode.

1           12.     The thin film transistor array panel of claim 1, wherein entire bottom surfaces of  
2     the data line and the drain electrode are disposed substantially on the semiconductor layer, the  
3     data line and the drain electrode have substantially the same planar shape as the semiconductor  
4     layer, and the semiconductor layer includes a portion that is not covered with the data line and  
5     the drain electrode and disposed between the source electrode and the drain electrode.

1           13.     The thin film transistor array panel of claim 1, wherein the first passivation layer  
2     and the pixel electrode covers an entire surface of the color filter.

1           14.     A liquid crystal display comprising:  
2         a first substrate;  
3         a first signal line disposed on the substrate;  
4         a second line disposed on the substrate and intersecting the first signal line;  
5         a thin film transistor connected to the first and the second signal lines;  
6         a color filter disposed on the first substrate;  
7         an insulating layer disposed on the color filter opposite the first and the second signal  
8     lines and the thin film transistor and having an opening exposing the color filter;  
9         a pixel electrode disposed on the color filter, connected to the thin film transistor,  
10      overlapping the insulating layer, and located substantially in the opening of the insulating layer;  
11      a second substrate facing the second substrate and spaced apart from the first substrate  
12      with a gap;  
13      a common electrode formed on the second substrate;  
14      a light blocking member disposed on the common electrode; and  
15      a liquid crystal layer filled in the gap between the first substrate and the second substrate.

1        15. The liquid crystal display of claim 14, wherein the insulating layer and the pixel  
2        electrode covers an entire surface of the color filter.

1        16. The liquid crystal display of claim 14, wherein the light blocking member  
2        includes a first portion maintaining the gap between the first substrate and the second substrate  
3        and a second portion having a thickness lower than the first portion.

1        17. The liquid crystal display of claim 14, further comprising a spacer disposed  
2        between the first substrate and the second substrate and maintaining the gap between the first  
3        substrate and the second substrate.

1        18. The liquid crystal display of claim 17, wherein the spacer is located on the thin  
2        film transistor.

1        19. The liquid crystal display of claim 14, wherein the liquid crystal layer has  
2        negative dielectric anisotropy and is subject to vertically alignment.

1        20. The liquid crystal display of claim 14, wherein the common electrode has a  
2        cutout.

1        21. A method of manufacturing a thin film transistor array panel, the method  
2        comprising:  
3           forming a plurality of gate lines on a substrate;  
4           forming a first insulating layer on the gate lines;

5 forming a semiconductor layer on the first insulating layer;  
6 forming a plurality of data lines and drain electrodes at least on the semiconductor layer;  
7 forming a plurality of color filters, each containing one of red, green and blue pigments;  
8 forming a second insulating layer at least on edges of the color filters, the second  
9 insulating layer disposed opposite the data lines; and  
10 forming a plurality of pixel electrodes on the color filters such that the pixel electrodes  
11 and the second insulating layer cover an entire surface of the color filters.

1 22. The method of claim 21, further comprising:

2 forming a third insulating layer on the data lines and the drain electrodes.

1 23. The method of claim 21, wherein the second insulating layer comprises a plurality

2 of portions disposed opposite the gate lines.